Process Design Kit for Flexible Hybrid Electronics

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Abstract— Flexible Electronics (FE) is emerging for wearables and low-cost internet of things (IoT) nodes benefiting from its low-cost fabrication and mechanical flexibility. Combining FE with thinned silicon chips, known as flexible hybrid electronics (FHE), can take advantages of both low-cost printed electronics and high performance silicon chips. To design a FHE system, the process design kit (PDK) offering the capabilities for circuit design, simulation and verification for both FE and silicon chips is needed. The key elements of FHE-PDK include technology files for design rule checking (DRC), layout versus schematic (LVS) and layout parasitics extraction (LPE), as well as SPICE-compatible models for flexible thin-film transistors (TFTs) and passive elements. Wafer scale measurements are used to validate our SPICE models and design rules are derived accordingly to assure a satisfactory yield. With FHE-PDK, circuit and system designers can therefore focus on design innovations and can rely on design tools to produce manufacturable designs.

I. Introduction

Flexible electronics is emerging as an alternative to conventional silicon electronics for applications such as wearable sensors, medical patches, bendable displays, foldable solar cells and disposable RFID tags [1][2][3]. Fig. 1 shows a test sample of a recent Pseudo-CMOS logic circuit with carbon nanotube (CNT) TFTs on a 1-μm thick plastic foil [1]. Unlike conventional silicon electronics that needs sophisticated billion-dollar foundry for manufacturing, flexible electronic circuits can be fabricated on thin and conformable substrates such as plastic films, with low-cost, high-throughput manufacturing methods such as ink-jet printing and roll-to-roll imprinting. The time-to-market as well as manufacturing cost can therefore be significantly reduced. Its flexible form factor also enables innovative designs for consumer electronics and biomedical applications [4][5].

However, several design challenges of flexible electronics must be addressed before their broad deployment to their products for next-generation IoT and wearable products. Table I compares the key characteristics of thin-film transistors (TFTs). Compared with crystalline-silicon metal-oxide-field-effect-transistor (MOSFET), TFTs often have a significantly slower operating speed and are less reliable. Due to material properties, TFTs are usually mono-type, either only p- or only n-type devices [6][7]. Making air-stable complementary TFT circuits is quite challenging or often requires heterogeneous

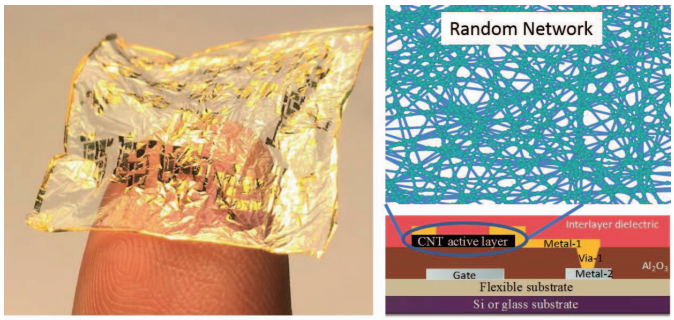

Fig. 1. (Left) A CNT-TFT logic circuit on a 1-μm thick plastic foil. (Right) Side view of a CNT-TFT [1].

process integration of two different TFT technologies. Existing CMOS design methodologies for silicon electronics, therefore, cannot be directly applied for designing flexible electronics. Other factors such as high supply voltages, large process variations, and lack of trustworthy TFT compact models for simulation also make designing large-scale TFT circuits a significant challenge.

Design often involves multiple levels of abstraction for ensuring minimum product re-spins, for protecting intellectual property and for creating a seamless flow from application, manufacturing, to product realization. Process Design Kits (PDK) has been a key reason for the great success of CMOS technology in last several decades. To enable the design of large-scale, highly integrated Flexible Hybrid Electronics (FHE), PDKs will be very critical. In contrast to the semiconductor industry where a single foundry is responsible for the entire manufacturing process, the FHE industry is fragmented-multiple manufacturers provide processes that cater to subsystem, but not the entire system. Unlike a wafer fab with an investment of billions of dollars, a combination from multiple foundries, each with an investment only in the order of a few million dollars, is used to realize the FHE. In addition, different foundries could provide different substrates such as PEN, PET, DuPont^{TM} Kapton, glass or paper to realize components such as resistors, inductors, capacitors, filters, antennas, sensors, batteries, etc. Such implementations will lead to greater deformation that any other systems today, and therefore addressing the associated mechanical, thermal, and electrical issues becomes critical. As technology evolves, new printing methods and materials will emerge with better properties. To

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TABLE I
COMPARISON BETWEEN DIFFERENT TFT TECHNOLOGIES

Device Type (TFT)	Amorphous Si	Metal-Oxide	SAM Organic	Polymer Organic	Carbon Nanotube
Process Temperature	$\sim 250°C$	$\sim 150°C$	$\sim 100°C$	Room temp.	Room temp.
Process Technology	Lithography	Roll-to-roll	Shadow mask	Ink-jet	Litho. & Shadow & R2R
Feature Size (μm)	8	5	50	50	25
Substrates	Glass/foil	Glass/foil	Foil	Foil	Foil
Device Type	N-type only	N-type only	Complementary	Complementary	Complementary
Supply Voltage (V)	20	10	2	40	2
Mobility (cm^2/Vs)	1	10	0.5	0.05	25

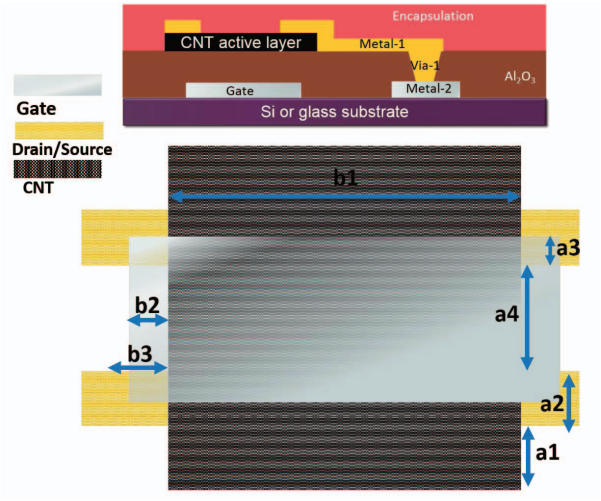

Fig. 2. (Top) Side view of a carbon nanotube transistor (CNT-TFT). (Bottom) Top view of a CNT-TFT including physical dimensions for DRC.

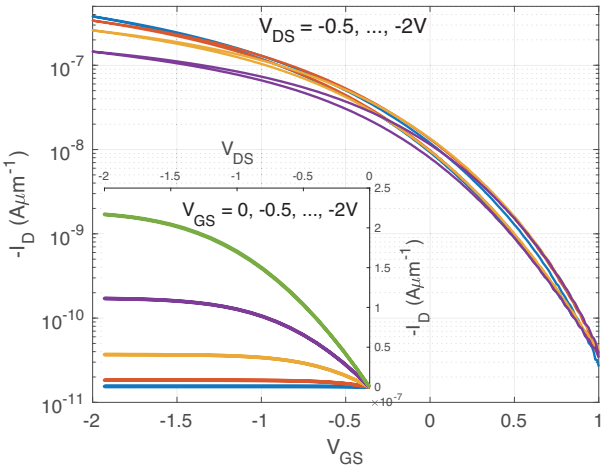

Fig. 3. Drain current versus gate voltages for a CNT-TFT.

enable seamless deployment of the FHE technologies, a framework is required where the design rules for each process can be captured, models can be developed and manufacturing details can be hidden, so that a designer can easily integrate various components into the system following a tool-assisted process. Needless to say, such a framework should be standardized and be compatible with commercial design environments using mainstream design tool suites. We currently collaborate with US Manufacturing Innovation Institute for Flexible Hybrid Electronics, *aka NextFlex*, to develop FHE-PDK to enable an open ecosystem for FHE design-manufacture-application.

In this paper, we first introduce the key devices our FHE-PDK is targeting which includes flexible carbon-nanotube thin-film transistors (CNT-TFTs) and passive elements such as resistors. The following sections provide more details about compact modeling and technology files for these emerging devices to be used for design, simulation, and physical verifications.

II. Flexible Carbon-Nanotube Devices

A. CNT Thin-Film Transistor

The cross section of a CNT-TFT is illustrated in Fig. 2, where a bottom gate structure is used. The bottom gate structure enables a denser CNT network for a better performance. Multiple layers of metal are connected using vias as the case for CMOS silicon chips, and currently up to four layers of metal are supported to enable higher design complexity for CNT-TFT circuits. The physical dimensions for design rule checking (DRC) are also labeled in Fig. 2 and currently down to 2-μm channel length is feasible using manual alignment and photolithography masks to directly fabricate TFTs on thin flexible substrates. For TFT technologies, there is only either n- or p-type of stable devices, but not both, as illustrated in Table I. CNT-TFT exhibits p-type characteristics and the fabrication of stable n-type CNT-TFTs remains a longstanding challenge. In this paper, we use p-type CNT-TFTs as an exemplar driver for FHE-PDK development.

A typical transfer curve of the drain current (I_{DS}) versus the gate voltage (V_{GS}) for a p-type CNT-TFT is shown in Fig. 3. Thanks to the high dielectric constant (~ 8) of the thin gate dielectric layer of Al_2O_3, a low supply voltage of 2 V is feasible to drive a CNT-TFT with a typical channel width of 125 μm and a length of 25 μm. A typical on-off current ratio is 10^5 to 10^6 for a CNT-TFT, and it often requires a positive gate voltage V_{GS} to turn off the device in the depletion mode.

B. CNT Resistor

Similar to a CNT-TFT, a CNT linear resistor is feasible by removing the gate terminal of a CNT-TFT to form a two-terminal CNT resistor on flexible substrates. A flexible CNT resistor ar-

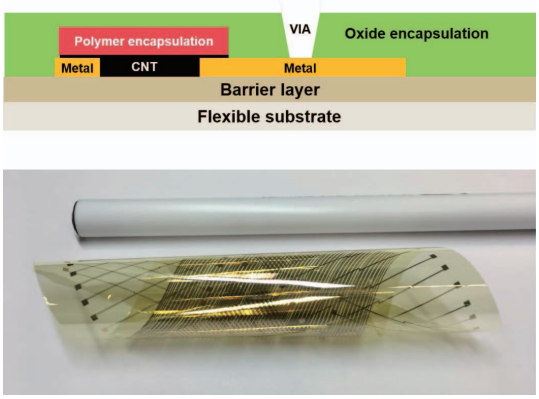

Fig. 4. (Top) Side view of a CNT resistor. (Bottom) Device photo of the CNT resistor array on a 10-μm thick polyamide foil.

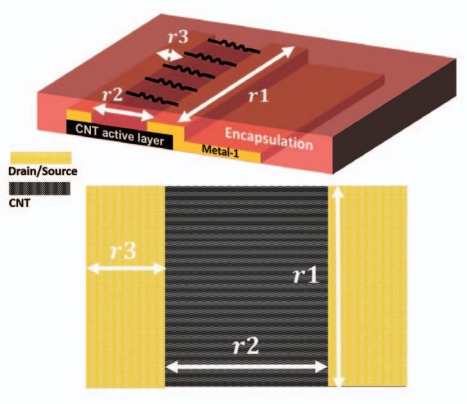

Fig. 5. Device dimension of a CNT resistor. r1 represents the device width W and r2 represent the device length L. r3 is the metal enclosure distance.

ray is shown in Fig. 4 including the side view of a CNT resistor. While the resistance values of a CNT linear resistor can be varied by width W and length L as indicated in Fig. 5, the sheet resistance is determined by the CNT material treatment. The current-voltage (I-V) relationship of the CNT resistor array is shown in Fig. 6, where the device width W is fixed at 40 μm and the device length L varies from 10 μm to 100 μm. These plots clearly indicate that CNT resistors have good linear relationship with 20-30% variations in their resistance values.

III. FHE-PDK Introduction and Compact Modeling

A. Introduction to the PDK

The PDK is a database for a specific technology, including devices properties and fabrication information, which can be stored in technology files and also expressed as SPICE/Verilog-A models. Illustrated in Fig. 7, the PDK provides all needed information for a typical circuit design flow from schematic simulation and physical verification to post-layout simulation.

Accurate SPICE/Verilog-A models are necessary for circuit simulation and design space exploration. In the technology file, technology information is stored and electrical properties and fabrication rules are defined as well. Specifically, it contains layer definitions, device definitions and physical/electrical

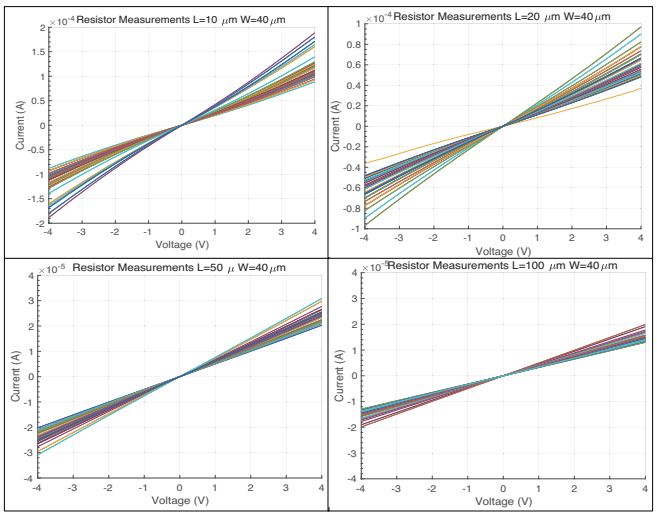

Fig. 6. Measured I-V characteristics of flexible CNT resistor array. The width is 40-μm and the length varies from 10-μm to 100-μm.

rules, which will be used for physical verification. Three procedures are required for verification: design rule checking (DRC), layout versus schematic (LVS) and layout parasitic extraction (LPE). DRC is used to verify whether the physical layout obeys the design rules predefined in the technology files, such as minimum widths, spacings and overlaps. Thus, a DRC-cleared design promises a high manufacturing yield. LVS is used to verify whether the physical layout, created for manufacturing, is equivalent to the schematic design, which is used for simulation. Finally, LPE is used to extract the parasitic devices, such as parasitic capacitors and resistors, which should be included for post-layout simulation to ensure high simulation fidelity.

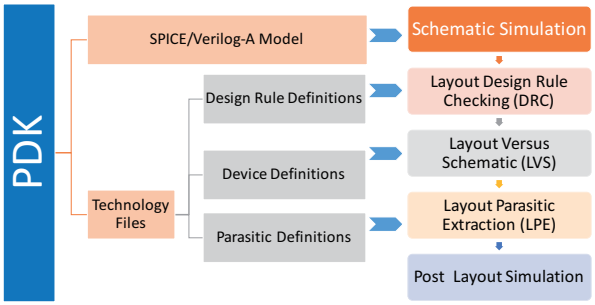

Fig. 7. Process Design Kit (PDK) provides necessary information for the circuit design.

B. Modeling for Flexible CNT-TFTs

In this section, we first introduce the CNT-TFT compact model which takes into account the mobility dependency on the gate voltage [8]. The model also includes the contact effect which improves the accuracy for predicting the CNT-TFT behavior.

CNT-TFT Compact Model There are multiple theories for the electrical transport mechanisms of CNT-TFTs, and the most accepted theories are based on charge drift in the presence of tail-distributed traps (TDTs) and variable range hopping (VRH) [9][10]. Both theories indicate the mobility dependency on the gate voltage [8][11]: $\mu \propto (V_G - V_{th})^{\gamma}$, $\gamma \geq 0$. V_{th} and γ are viewed as device parameters and complex deductions for V_{th} and γ are omitted in our analysis. The derived CNT-TFT compact model is shown in Eqs. (1)-(3), based on the well-established concept for charge drift (the deduction details can be found in [8][12]), where a limiting function $f_{\text{lim}}(x, A) = A\ln(1 + \exp(\frac{x}{A}))$ is used to represent the transition from the sub-threshold region to the above-threshold region. Limiting functions have been widely used for compact modeling to provide smooth transition between different regions [12].

$$I_D = k(f(V_G, V_S)^{\gamma+2} - f(V_G, V_D)^{\gamma+2})(1 + \lambda V_{DS}) \quad (1)$$

$$f(V_G, V) = VSS\ln[1 + \exp(\frac{V_G - V_{th} - V)}{VSS}] \quad (2)$$

$$k = \frac{W\mu_0 C_{ox}}{L(\gamma + 2)} \quad (3)$$

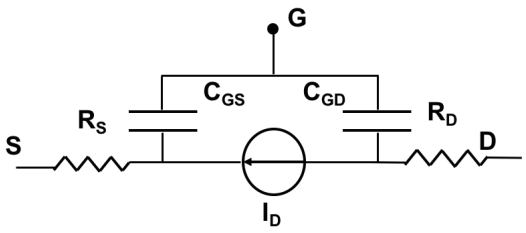

Fig. 8. The CNT-TFT compact model.

Although the model is derived for n-type devices, we can easily get the p-type model by changing the polarities of voltages and currents. The model described by Eqs. (1)-(3) doesn't include the contact resistance R_C, which is caused by the current injection at the source and drain electrodes [8]. To take into account the effect of contact resistance, two series resistors are added to the CNT compact model, as shown in Fig. 8. With the contact resistance included, this model achieves sufficient accuracy matching the measured behavior of the CNT-TFT. The fitting results and measurements are shown in Fig. 9, which clearly indicates that the CNT compact model can accurately predict CNT-TFT behaviors.

Parameter Extraction To characterize the variations of CNT-TFTs, we perform nonlinear least-square optimization to automatically extract the parameters for 52 printed CNT-TFTs. Device parameters W, L and C_{ox} are directly obtained, and thus six parameters in the proposed model need to be extracted: V_{th}, γ, VSS, μ, R_C and λ. The extraction process involves two steps: 1) Derive an initial value for each of these parameters. For example: V_{th} is extracted as the x-axis intercept of the square root of the transfer characteristic in the saturation region and VSS is determined based on the slope in the sub-threshold region. For fitting parameters like γ and

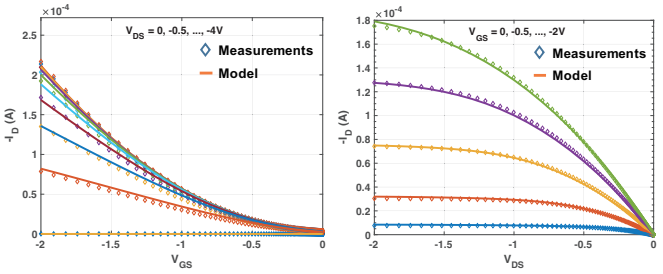

Fig. 9. Model validation for $I - V$ curves.

λ, an appropriated guess and lower/upper bounds would be derived. 2) Based on the extracted or guessed initial values, nonlinear least-square optimization is performed to minimize the defined error function for deriving the final values for these parameters. To achieve fitting results with greater accuracy, an error criteria including both current and conductance errors are used [12], as shown below:

$$E_I = \sum_{j=1}^{K}\{w_{I_{D_j}}(\frac{\widehat{I_{D_j}} - I_{D_j}}{|\widehat{I_{D_j}}| + |I_{D_j}|})^2 + w_{g_{o_j}}(\frac{\widehat{g_{o_j}} - g_{o_j}}{|\widehat{g_{o_j}}| + |g_{o_j}|})^2\} \quad (4)$$

$$g_o = \partial I_D / \partial V_D \quad (5)$$

Here, w_{I_D} and w_{g_o} represent the weights for current error and conductance error respectively and they are set to have the same value as the default. This error function is expressed in terms of percentage error and helps automatically reject noisy data at a low bias level.

TABLE II
PARAMETERS EXTRACTED FROM 52 FABRICATED CNT-TFTS

Model Parameter	Notation	[μ, σ] Unit
Channel Length	L	[25, -] um
Channel Width	W	[125, -] um
Gate Unit Capacitance	C_{ox}	[200, -] nF/cm^2
Threshold voltage	V_{th}	[0.5, 0.102] V
Sub-threshold Swing	SS	[0.28, 0.0388] V/dec
Effective Mobility	μ_0	[25.69, 0.19] cm^2/Vs
Contact Resistance	R_C	[1531, 291] Ω
Channel Length Modulation	λ	[0.064, 0.0185] V^{-1}
Factor of Gate Dependent mobility	γ	[0.20, 0.116] (-)

We extracted all parameters for 52 fabricated CNT-TFTs which are summarized in Table II. The table also includes the mean value μ and standard deviation σ, where a Gaussian distribution is assumed for device variations for each parameter.

C. Modeling for Flexible Resistors

In addition to TFTs, the CNT film can also be used to produce resistors, whose fabrication process is compatible with that of CNT-TFT. With both passive components and active

TFTs being available, circuits with a broader range of functionality can be built.

Flexible Resistor Modeling Modeling for the resistors is straightforward and a simple resistor model is used in our PDK, as shown in Fig. 10. For simplicity, the parasitic capacitor and inductor are ignored. The model contains an intrinsic part and an external part, where the external part is induced by the imperfect contact between the CNT film and the connection metal. Therefore, the total resistance R_{total} of the flexible resistor is composed of contact resistance $R_c = R_{cs} + R_{cd}$ and channel resistance R_{ch}. Here, R_{ch} is the sheet resistance of the channel and R_{sd} is the unit width contact resistance.

$$R_{toal} = \frac{R_c}{W} + \frac{R_{ch}L}{W} \tag{6}$$

Eq. (6) indicates that the R_{total} is a linear function of L if W is kept as a constant. $R_c/W = 4.78K\Omega$ is the intersection when $L = 0$, and $R_{ch}/W = 2.46K\Omega$ is the slope, as illustrated in Fig. 10.

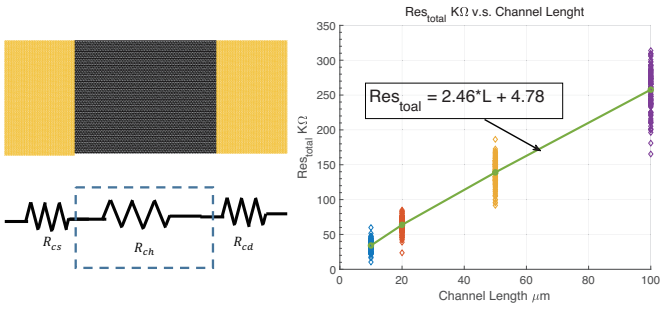

Fig. 10. Flexible resistor analysis based on ≈ 500 fabricated devices with $L = 10,\ 20,\ 50,\ 100\ \mu m$ and $W = 40\ \mu m$.

IV. Physical Verification Implementation

Physical verification is used to avoid fabricating incorrect masks and to insure a satisfactory manufacturing yield and performance [13]. Electronics Design Automation (EDA) tools have been developed and widely used for CMOS chips, which can handle extremely complex circuity with millions of transistors and more than 10 physical layers. The best approach for FE verification is to take advantage of available CMOS-centric EDA tools and focus on expressing the relevant information of our CNT technology into formats that can be directly recognized by commercial tools, as indicated in Fig. 11.

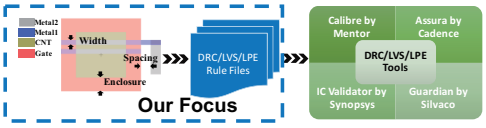

Fig. 11. DRC, LVS and LPE Flow.

In the following, we introduce how the verification engine works and several key steps will be discussed in details. For illustration purposes, a typical physical verification rule structure is provided as below:

Physical Verification Rule Structure

Load Technology files: {
Layer Assignments;
Define Material Properties;
Define Physical Constraints}
DRC Statements : {
Local Layer Definitions;
Layer Derivations;
Rule Check Comments}
LVS Statements : {
Device Recognition;
Layout Netlist Generating;
Netlists Equivalent Checking}
LPE Statements: {
Parasitic Recognition;
Parasitic Netlist Generating}

A. Design Rule Checking (DRC)

DRC verifies whether the designed mask obeys the fabrication constraints, such as minimum widths, spacings and overlaps. According to their geometry representations, mainstream DRC approaches can be categorized as: polygon, raster (bitmap) and edge based methods [14][15][16]. Despite the representation differences, the checking sequence is exactly the same: 1) local layer definition, 2) layer derivation, and 3) rule checking. The local layer definition is used to derive the critical regions in a layout. For layer derivation, it performs the boolean operation of basic layers, as shown in Fig. 12, and constructs useful regions. Thus, we can easily conduct rule checking using basic checking statements, as illustrated in Fig. 13.

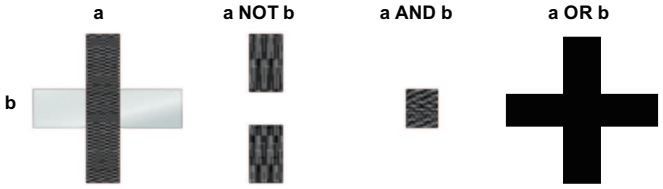

Fig. 12. Common boolean operations of layer a and b. Boolean operations: NOT, AND and OR are demonstrated.

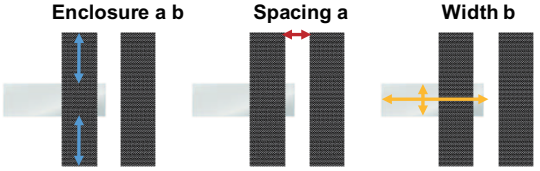

Fig. 13. Common checking statements: enclosure, spacing and width.

The basic boolean operations of the polygon are shown in Fig. 12. For illustration purposes, only most common and use-

ful operations are introduced. These operations find critical combinations of layers that comprise devices and connections. For example, the 'Source/Drain' layer can be constructed as boolean AND of Metal and CNT layers. The combination of boolean operations (AND, NOT, OR, etc.) can generate all desired regions to facilitate the following rule checking task. Using CNT-TFT as an example, we illustrate how to use boolean combinations to derive critical regions of a CNT-TFT as below:

Exemplary Layer Derivation of CNT-TFTs				
Temp	=	CNT	AND	Gate
Channel	=	Temp	NOT	Metal
SD	=	Metal	AND	CNT
....				

Once critical regions are derived, it is straightforward to check the basic constraints: spacing, width and enclosure, as shown in Fig. 13.

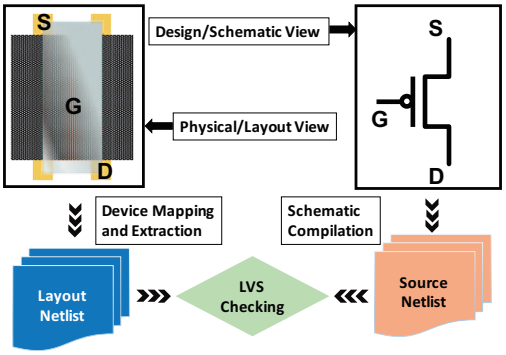

Fig. 14. LVS principles and procedures.

B. Layout Verses Schematic (LVS)

LVS verifies the physical implementation by comparing a netlist extracted from a circuit layout to a schematic netlist that is assumed to be correct [17]. Basic procedures of the LVS are illustrated in Fig. 14, where netlists are extracted from both the schematic and the layout. Then, both netlists are converted into graphs and graph isomorphism is used to check their equivalence [18][19].

For the schematic view, it is straightforward to generate the netlist. However, for the layout view, we have to define the device recognition rules, which will be used to extract and generate the layout netlist. Also, device properties, such as a transistor's length and width, should be extracted as well. High level syntax of device recognition for CNT-TFTs is provided as below:

Device Recognition Example
CNT-TFT device recognition : Gate ⇔(G) SD ⇔(S) SD ⇔(D)
[**Property extraction:** L, W, AS, AD
W = Length(Channel)
L = Area(Channel)/W
AS = Area(SD)/2
AD = Area(SD)/2]

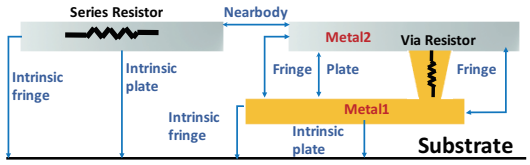

Fig. 15. Different types of parasitic capacitors and resistors.

C. Layout Parasitic Extraction (LPE)

Parasitics in flexible electronics could be significant due to its low cost processes. Therefore, it is essential to extract the parasitic resistors and capacitors for inclusion in post-layout simulation. As shown in Fig. 15, the parasitic capacitors contain the intrinsic capacitors, formed between conducting layers and the substrate, and coupling capacitors, formed by nearby layers. Parasitic resistors exist in both the conduction layers and connection vias. After parasitic extraction and parasitic netlist generation, post-layout simulation can be performed for more accurate simulation results. Abstract description of parasitic recognition is provided as below:

Parasitic Recognition Example
Parasitic capacitor recognition : intrinsic or coupling
[**Property extraction:** C
C = C_{plate} * Area()+ C_{fringe} * Perimeter()]
Parasitic resistor recognition : conducting layers or vias
[**Property extraction:** R
R = R_{Sheet} * Length()/Width()]

V. Conclusion

In this paper, we introduce CNT-based flexible electronics and illustrate how PDK can assist the design process of a FHE system involving schematic design, physical layout and post-layout simulation. We have developed compact models for both TFTs and resistors of our target CNT technology, which have been thoroughly validated based on measurement results of fabricated devices. Also, models and procedures for physical verification are included to enable the use of existing EDA tools for ensuring manufacturability. We believe this fully functional FHE-PDK can facilitate innovative design of large-scale FHE systems and potentially trigger a fabless design business model for the FHE industry.

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