

Connexions

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MOS Regimes

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Summary: Introducing the Sah equation, and discussing some properties of this equation.

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This equation looks a lot like the I-V characteristics of a resistor! I_d is simply proportional to the drain voltage V_{ds} . The proportionality constant depends on the dimensions of the device, W and L as they intuitively should. The current increases as the transistor gets wider, it decreases as it gets longer. It also depends on c_{ox} and μ_s , and on the difference between the gate voltage and the threshold voltage V_T . Note that if we adjust V_{gs} we can change the slope of the I-V curve. We have made a voltage-controlled resistor!

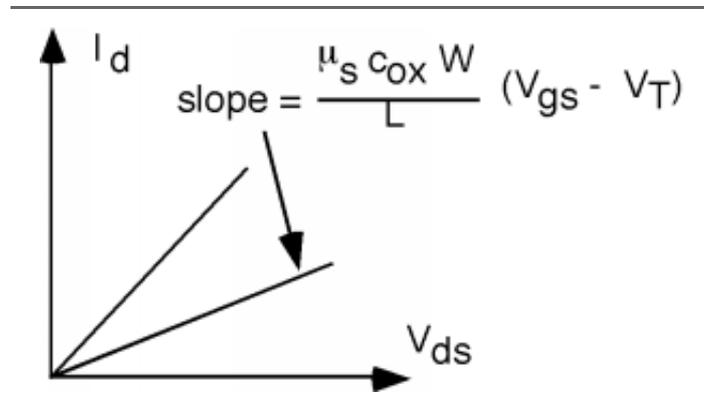


Figure 1: The MOSFET I-V in the linear regime

Caution is advised with this result however, because we have overlooked something quite important. Let's go back to our picture of the gate and the batteries involved in the operation of the MOS transistor. Here we have explicitly shown the channel as a black band and we have introduced a new quantity, $V_c(x)$, the voltage along the channel, and a coordinate x , which tells us where we are on the channel relative to the source and drain. Note that once we apply a drain source potential, V_{ds} , the potential in the channel $V_c(x)$ changes with distance along the channel. At the source end, $V_c(0) = 0$, as the source is grounded. At the drain end, $V_c(L) = V_{ds}$. We will define a voltage V_{gc} which is the potential difference between the gate voltage and the voltage in the channel.

$$V_{gc}(x) \equiv V_{gs} - V_c(x)$$

(1)

Thus, V_{gc} goes from V_{gs} at the source end to $V_{gs} - V_{ds}$ at the drain end.

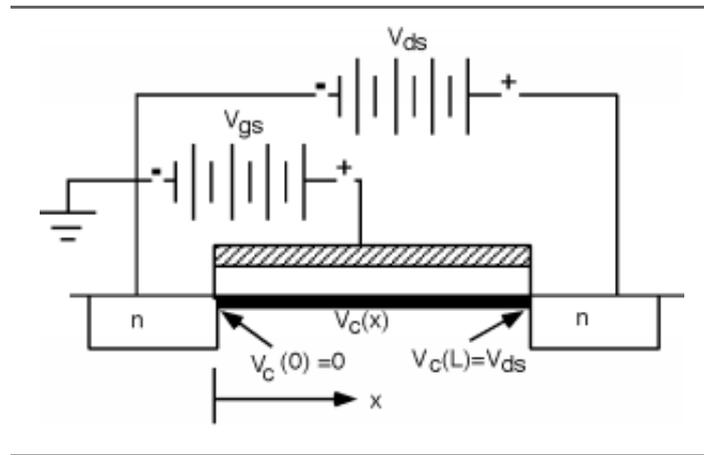


Figure 2: Effect of V_{ds} on channel potential

The net charge density in the channel depends upon the potential difference between the **gate and the channel at each point along the channel**, not just $V_{gs} - V_T$. Thus we have to modify [the equation of another module](http://cnx.org/content/m1023/latest/#eqn30) (<http://cnx.org/content/m1023/latest/#eqn30>) to take this into account

$$\begin{aligned} Q_{\text{chan}} &= c_{\text{ox}} (V_{gc}(x) - V_T) \\ &= c_{\text{ox}} (V_{gs} - V_c(x) - V_T) \end{aligned} \quad (2)$$

This, in turn, modifies the [integral relation](http://cnx.org/content/m1023/latest/#eqn34) (<http://cnx.org/content/m1023/latest/#eqn34>) between I_d and V_{gs} .

$$\int_0^{V_{ds}} \mu_s c_{\text{ox}} (V_{gs} - V_T - V_c(x)) W dV_c(x) = \int_0^L I_d dx \quad (3)$$

[Equation 3](#) (#eqn38) is only slightly harder to integrate than the one before (Now what **is** the integral of $x dx$), and so we get for the drain current

$$I_d = \frac{\mu_s c_{\text{ox}} W}{L} \left((V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad (4)$$

This equation is called the **Sah Equation** after C.T. Sah, who first described the MOS transistor operation this way back in 1964. It is very important because it describes the basic behavior of the MOS transistor.

Note that for small values of V_{ds} , [a previous equation](http://cnx.org/content/m1023/latest/#eqn35) (<http://cnx.org/content/m1023/latest/#eqn35>) and [Equation 4](#) (#eqn39) will give us the same $I_d - V_{ds}$ behavior, because we can ignore the V_{ds}^2 term in [Equation 4](#) (#eqn39). This is called the **linear regime** because we have a straight-line relationship between the drain current and the drain-source voltage. As V_{ds} starts to get larger however, the squared term will begin to kick in and the plot will start to curve over. Obviously, something is causing the current to drop off as V_{ds} gets larger. This is because the voltage difference between the gate and the channel is becoming less, which means there is less charge in the channel to provide conduction. We can graphically show this by making the channel layer look thinner as we move from the source to the drain. [Equation 4](#) (#eqn39), and in fact, [Figure 3](#) (#fig18) would make us think that if V_{ds} gets large enough, that the drain current I_d should actually start decreasing again, and maybe even become negative!. This does not seem very intuitive, so let's take a look in more detail at the place where I_d becomes a maximum. We can define V_{dsat} as the source-drain voltage where I_d becomes a maximum. We can find this by taking the derivative of I_d with respect to V_{ds} and setting the derivative to 0.

$$\frac{d}{dV_{ds}} (I_d) = 0$$

$$= \frac{\mu_s c_{ox} W}{L} (V_{gs} - V_T - V_{dsat})$$
(5)

On dropping constants:

$$V_{dsat} = V_{gs} - V_T$$
(6)

Rearranging this equation gives us a little more insight into what is going on.

$$V_{gs} - V_{dsat} = V_T$$

$$= V_{gc} (L)$$
(7)

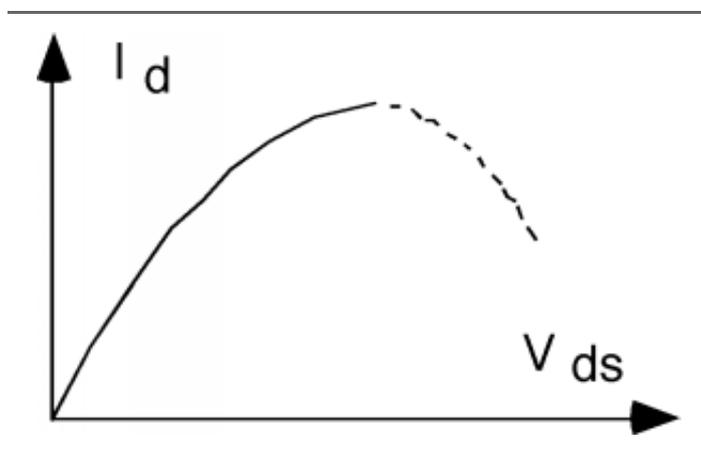


Figure 3: I-V characteristics showing turn-over

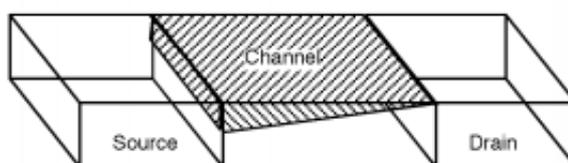


Figure 4: Effect of V_{ds} on the channel

At the drain end of the channel, when V_{ds} just equals V_{dsat} , the difference between the gate voltage and the channel voltage, $V_{gc} (L)$ is just equal to V_T , the threshold voltage. Any further increase in V_{ds} and the difference between the gate and the channel (**in the channel region just near the drain**) will drop below the threshold voltage. This means that when V_{ds} gets bigger than V_{dsat} , the channel just near the drain region disappears! We no longer have sufficient voltage between the gate and the channel region to maintain an inversion layer, so we simply revert to a depletion condition. This is called **pinch off**, as seen in [Figure 5 \(#fig20\)](#).

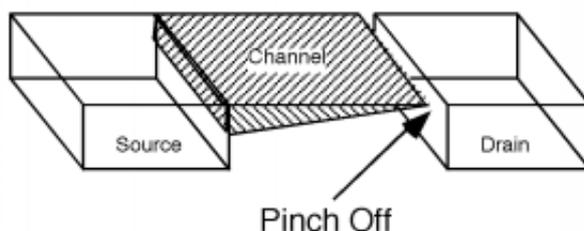


Figure 5: Channel in pinch-off

What happens to the drain current when we hit pinch off? It looks like it might go to zero, but that is not the right answer! Although there is no active channel in the pinch-off region, there is still silicon - it just happens to be depleted of all free carriers. There is an electric field, going from the drain to the channel, and any electrons which move along the channel to the pinch-off region are sucked across by the field, and enter the drain. This is just like the current that flows in the reverse saturation condition of a diode. There are no free carriers in the depletion region of the diode, yet I_{sat} **does** flow across the junction region.

Under pinch-off conditions, further increases in V_{ds} , does not result in more drain current. You can think of the pinched-off channel as a resistor, with a voltage of V_{dsat} across it. When V_{ds} gets bigger than V_{dsat} , the excess voltage appears across the pinch-off region, and the voltage across the channel remains fixed at V_{dsat} . If the channel keeps the same charge, and has the same voltage across it, then the current through the channel (and into the drain) will remain fixed, at a value we will call I_{dsat} .

There is one other figure which sometimes helps in seeing what is going on. We will plot potential energy for an electron, as it traverses across the channel. Since the source is at zero potential and the drain is at $+V_{\text{ds}}$, an electron will lose potential energy as it flows from the source to the drain. [Figure 6](#) (#fig21) shows some examples for various values of V_{ds} :

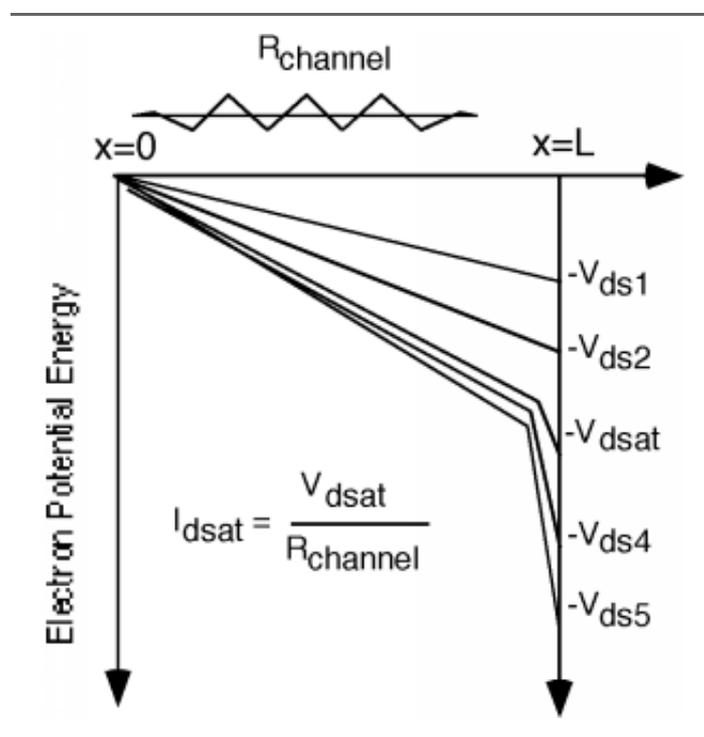


Figure 6: Electron potential energy drop going from source to drain.

For the first two drain voltages, V_{ds1} and V_{ds2} , we are below pinch-off, and so the voltage drop across $R_{channel}$ increases as V_{ds} increases, and hence, so does I_d . At V_{dsat} , we have just reached pinch-off, and we are starting to see the "high field" depletion region begin to develop. Since electric field is just the derivative of the potential, the slope of curves in [Figure 6 \(#fig21\)](#) gives you an idea of how big the electric field will be. For further increases in V_{ds} , V_{ds4} and V_{ds5} all of the additional voltage just shows up as a high field drop at the end of the channel. The voltage drop across the conducting part of the channel stays fixed (more or less) at V_{dsat} and so the drain current stays more or less fixed at I_{dsat} .

Substituting the expression for V_{dsat} into the expression for I_d we can get an expression for I_{dsat}

$$I_{dsat} = \frac{\mu_s c_{ox} W}{2 L} (V_{gs} - V_T)^2 \quad (8)$$

We can define a new constant, k , where

$$k = \frac{\mu_s c_{ox} W}{L} \quad (9)$$

So that

$$I_{dsat} = \frac{k}{2} (V_{gs} - V_T)^2 \quad (10)$$

What this means for [Figure 3 \(#fig18\)](#) is that when V_{ds} gets to V_{dsat} , we simply hold I_d fixed from then on, with a value of I_{dsat} . For different values of V_g , the gate voltage, we are going to have a different $I_d - V_{ds}$ curve, and so once again, we end up with a family of "characteristic curves" for the MOSFET. These are shown in [Figure 8 \(#fig23\)](#).

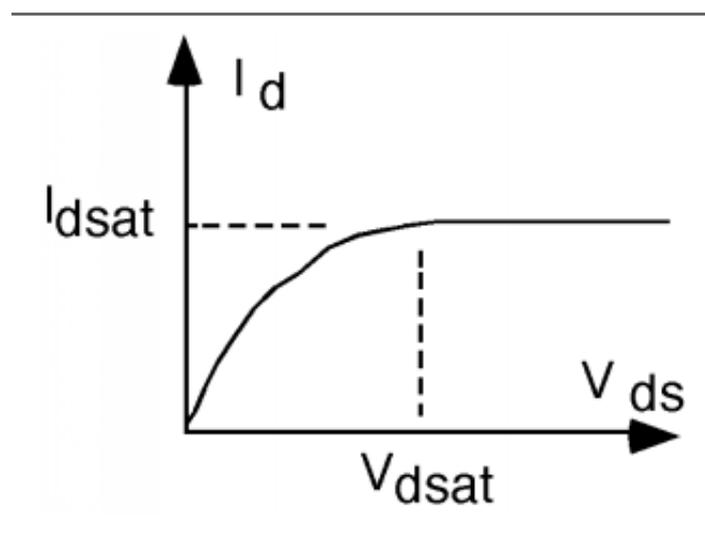


Figure 7: Complete I-V curve for the MOSFET

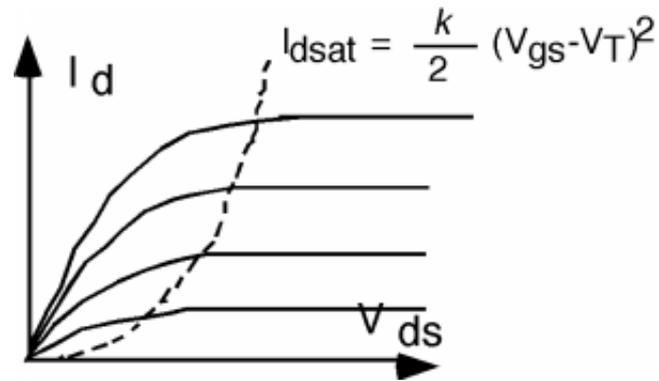


Figure 8: Characteristic curves for a MOSFET

This also gives us a fairly easy way in which to "sketch" a set of characteristic curves for a given device. Suppose we have a MOS field effect transistor which has a threshold voltage of 2 volts, a width of 10 microns, and a channel length of 1 micron, an oxide thickness of 150 angstroms, and a surface mobility of 400

$\frac{c}{V \text{ sec}}$. using $\epsilon_{\text{ox}} = 3.3 \times 10^{-13} \frac{F}{\text{cm}}$, we get a value of $2.2 \times 10^{-7} \frac{F}{c}$ for c_{ox} . This then makes k have a value

of

$$\begin{aligned}
 k &= \frac{\mu_s c_{\text{ox}} W}{L} \\
 &= \frac{400 \times 2.2 \times 10^{-7} \text{ } 10}{1} \\
 &= 8.8 \times 10^{-4} \frac{\text{amp}}{\text{volt}^2}
 \end{aligned} \tag{11}$$

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